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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,067	09/28/2000	Samson X. Huang	884.326US1	2844

7590 12/18/2002

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EXAMINER
ALPHONSE, FRITZ

ART UNIT	PAPER NUMBER
2675	4

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/675,067	Huang
Examiner	**Art Unit**
Fritz Alphonse	2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 20, 2000* .

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 2, 9, 10, 12, 14-16, and 19* is/are rejected.

7) ☒ Claim(s) *3-8, 11, 13, 17, 18, and 20-23* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 9-10, 14, are rejected under 35 U.S.C. 102(b) as being anticipated by Ferris (U.S. Pat. No. 5,163,023).

Regarding claim 1, Ferris (figs. 1-5) teaches about an apparatus for repairing memory circuit comprising: a memory device (1) having a memory device input data bus (see figure 1) including a least significant bit and a plurality of non-least significant bits (col. 2, lines 52-56). Ferris teaches about a repair router (i.e., routing circuitry 8) having a repair router input data bus including a least significant bit and a plurality of non-least significant bits (see fig. 1), and a repair router output data bus coupled to the memory device input data bus (fig. 4; col. 2, lines 27-51; see abstract), the repair router having internal routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the least significant bit of the memory device input data bus (col. 5, lines 8-25).

As to claim 2, Ferris (fig. 1) discloses an apparatus, wherein the plurality of non-least significant bits includes a next-to-least significant bit; and a repair router further includes additional

repair routing circuitry to route any of the non-least significant bits to the next-to-least significant bit.

As to claim 9, the claim differs from claim 1 only in that the limitation "a plurality of addressable memory locations, each including a least significant bit and a plurality of non-least significant bits" are added. However, Ferris teaches about a memory array having a plurality of memory cells (col. 2, lines 10-20) including least and non-least significant bits.

As to claim 10, Ferris (fig. 1) discloses a memory device, wherein the plurality of addressable memory locations are arranged into a plurality of address ranges; and the first repair router further includes address decoding circuitry to decode each of the plurality of address ranges.

As to claim 12, Ferris discloses a memory device wherein the repair router is configured to route a specific non-least significant bit to the least significant bit of the plurality of addressable memory locations when a problem exists with the specific non-least significant bit in at least one of the plurality of addressable memory locations (col. 2, lines 28-56).

As to claim 14, the claim has substantially the limitations of claim 1. Therefore, it is analyzed as previously discussed in claim 1 above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferris in view of Lindsay (U.S. Pat. No. 6,330,693).

As to claim 15, the claim differs from claim 1 by the additional limitations "a display device having an array of pixels; a memory having a plurality of addresses, each of the plurality of addresses corresponding to one pixel in the array of pixels".

However in the same field of endeavor Lindsay (figs. 1, 2) shows a display device (120) having an array of pixels; a memory (134) having a plurality of addresses (135), each of the plurality of addresses (135) corresponding to one pixel in the array of pixels (col. 3, lines 46-52; col. 7, lines 12-31; fig. 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the testing memory devices as disclosed by Lindsay. Doing so would provide a much more faster repair router circuitry.

As to claim 16, the claim has substantially the limitations of claim 15. Therefore, it is analyzed as previously discussed in claim 15 above.

As to claim 19, Ferris (fig. 1) discloses a display system wherein the plurality of addresses are arranged in a plurality of groups; and the repair router includes routing circuitry to utilize the least significant bits of each of the plurality of groups separately.

Allowable Subject Matter

5. Claims 3-8, 11, 13, 17-18, and 20-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed on 9/23/02 have been fully considered but they are not persuasive.

Applicant argues that Ferris's routing circuitry does not teach the ability to route any of the non-least significant bit as claimed in claim 1.

The examiner respectfully disagrees with that statement because Ferris (col. 2, lines 52-56) clearly provides the ability to route the non-least significant bit as claimed in claim 1.

As to argument that Ferris does not disclose, teach, or suggest the subject matter of claim 9, including for example, "the first router including circuitry to route any of the plurality of non-least significant bits of the repair router including data bus to the least significant bit of at least one of the plurality of addressable memory locations."

In that regard, the examiner disagrees. Ferris's art relates to a memory circuit in which a faulty column can be replaced in order to repair the circuit. Therefore, Ferris teaches about a routing circuitry which is capable to repair the faulty memory. That is the same problem that the applicant wants to be solved.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703)308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT"

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse whose telephone number is (703) 308-8534.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached on (703) 305-9720.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

F. Alphonse

Art Unit: 2675

December 16, 2002

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600